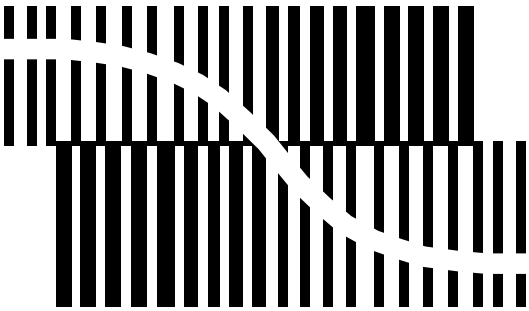
DATA SHEET



TDA1305T

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

Preliminary specification
Supersedes data of September 1994
File under Integrated Circuits, IC01

1995 Dec 08

Philips
Semiconductors

PHILIPS

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

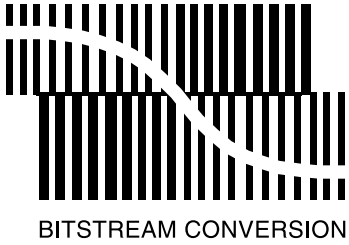
TDA1305T

FEATURES

- Easy application
- $16f_s$ Finite-duration Impulse-Response (FIR) filter incorporated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus serial input format (at $f_{sys} = 256f_s$) or LSB fixed 16, 18 or 20 bits serial input mode (at $f_{sys} = 384f_s$)
- Slave-mode clock system
- Cascaded 4-stage digital filter incorporating 2-stage FIR filter, linear interpolator and sample-and-hold
- Smoothed transitions before and after muting (soft mute)
- Digital de-emphasis filter for three sampling rates of 32 kHz, 44.1 kHz and 48 kHz
- 12 dB attenuation via the attenuation input control
- Double speed mode
- 2nd order noise shaper
- 96 ($f_{sys} = 384f_s$) or 128 ($f_{sys} = 256f_s$) times oversampling in normal speed mode
- 48 ($f_{sys} = 384f_s$) or 64 ($f_{sys} = 256f_s$) times oversampling in double speed mode
- Bitstream continuous calibration concept
- Small outline SO28 package
- Voltage output 1.5 V (RMS) at line drive level
- Low total harmonic distortion
- No zero crossing distortion
- Inherently monotonic
- No analog post filtering required
- Superior signal-to-noise ratio
- Wide dynamic range (18-bit)
- Single rail supply (3.4 to 5.5 V).

GENERAL DESCRIPTION

The TDA1305T is a new generation of filter-DAC which features a unique combination of bitstream and continuous calibration techniques. The converter functions as a bitstream converter for low signals while large signals are generated using the dynamic continuous calibration technique, thus resulting in low power consumption, small chip size and easy application.



The TDA1305T is a dual CMOS DAC with up-sampling filter and noise shaper. The combination of high oversampling up to $16f_s$, 2nd order noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1305T supports the I^2S-bus data input mode with word lengths of up to 20 bits (at $f_{sys} = 256f_s$) and the LSB fixed serial data input format with word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). Four cascaded FIR filters increase the oversampling rate to 16 times. A sample-and-hold function increases the oversampling rate to 96 times ($f_{sys} = 384f_s$) or 128 times ($f_{sys} = 256f_s$). A 2nd order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special date coding. This ensures an extremely high signal-to-noise ratio, superior dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage. Externally connected capacitors perform the required 1st order filtering so that no further post filtering is required.

The unique combination of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a single filter-DAC with 18-bit dynamic range, high linearity and simple low cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1305T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
I_{DDO}	operating amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V	1.425	1.5	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB signal level	–	–44	–40	dB
			–	0.63	0.1	%
		at –60 dB signal level; A-weighted	–	–46	–	dB
			–	0.5	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting; at code 00000H	100	108	–	dB
BR_{ns}	input bit rate at data input	f_s = 48 kHz; normal speed	–	–	3.072	Mbits
BR_{ds}	input bit rate at data input	f_s = 48 kHz; double speed	–	–	6.144	Mbits
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply.

BLOCK DIAGRAM

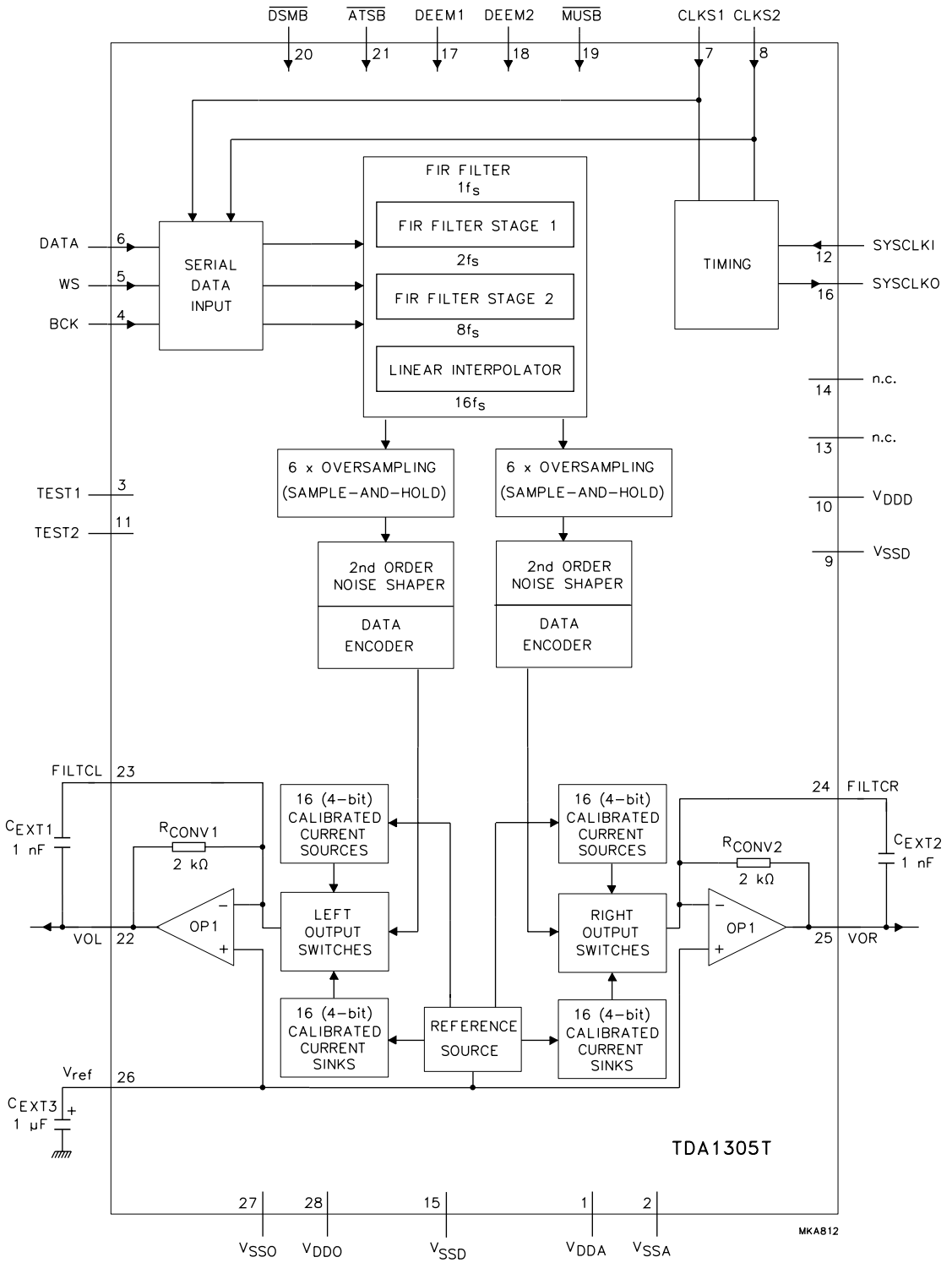


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
V_{SSA}	2	analog ground
TEST1	3	test input; pin should be connected to ground (internal pull-down resistor)
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock selection 1 input
CLKS2	8	clock selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input; pin should be connected to ground (internal pull-down resistor)
SYSCLKI	12	system clock input
n.c.	13	not connected (this pin should be left open-circuit)
n.c.	14	not connected (this pin should be left open-circuit)
V_{SSD}	15	digital ground
SYSCLKO	16	system clock output
DEEM1	17	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
DEEM2	18	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
$\overline{MUSB}$	19	mute input (active LOW)
$\overline{DSMB}$	20	double-speed mode input (active LOW)
$\overline{ATSB}$	21	12 dB attenuation input (active LOW)
VOL	22	left channel output
FILTCL	23	capacitor for left channel 1st order filter function should be connected between pins 22 and 23
FILTCR	24	capacitor for right channel 1st order filter function should be connected between pins 25 and 24
VOR	25	right channel output
V_{ref}	26	internal reference voltage for output channels ($0.5V_{DD}$)
V_{SSO}	27	operational amplifier ground
V_{DDO}	28	operational amplifier supply voltage

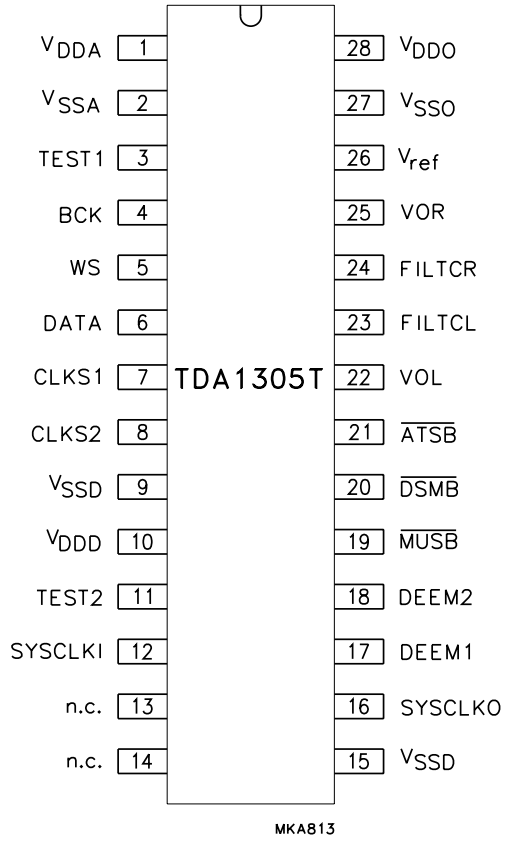


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1305T CMOS digital-to-analog bitstream converter incorporates an up-sampling filter and noise shaper which increase the oversampling rate of $1f_s$ input data to $96f_s$ ($f_{sys} = 192f_s$) or $128f_s$ ($f_{sys} = 256f_s$) in the normal speed mode. In the double speed mode the oversample rate of $1f_s$ input data is increased to $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$). This oversampling, together with the 5-bit DAC, enables the filtering required for waveform smoothing and out-of-band noise reduction to be achieved by simple 1st order analog post filtering.

System clock and data input format

The TDA1305T accommodates slave mode only, this means that in all applications the system devices must provide a system clock of 256 or $384f_s$ (f_s = 32, 44.1 or 48 kHz). The system frequency is selectable by means of pin CLKS1 and pin CLKS2. The SYSCLKO output (pin 16) provides the system clock for external use.

The TDA1305T supports the following data input modes:

- I^2S-bus with data word lengths of up to 20 bits (at $f_{sys} = 256f_s$).
- LSB fixed serial format with data word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). As this format idles on the MSB it is necessary to know how many bits are being transmitted.

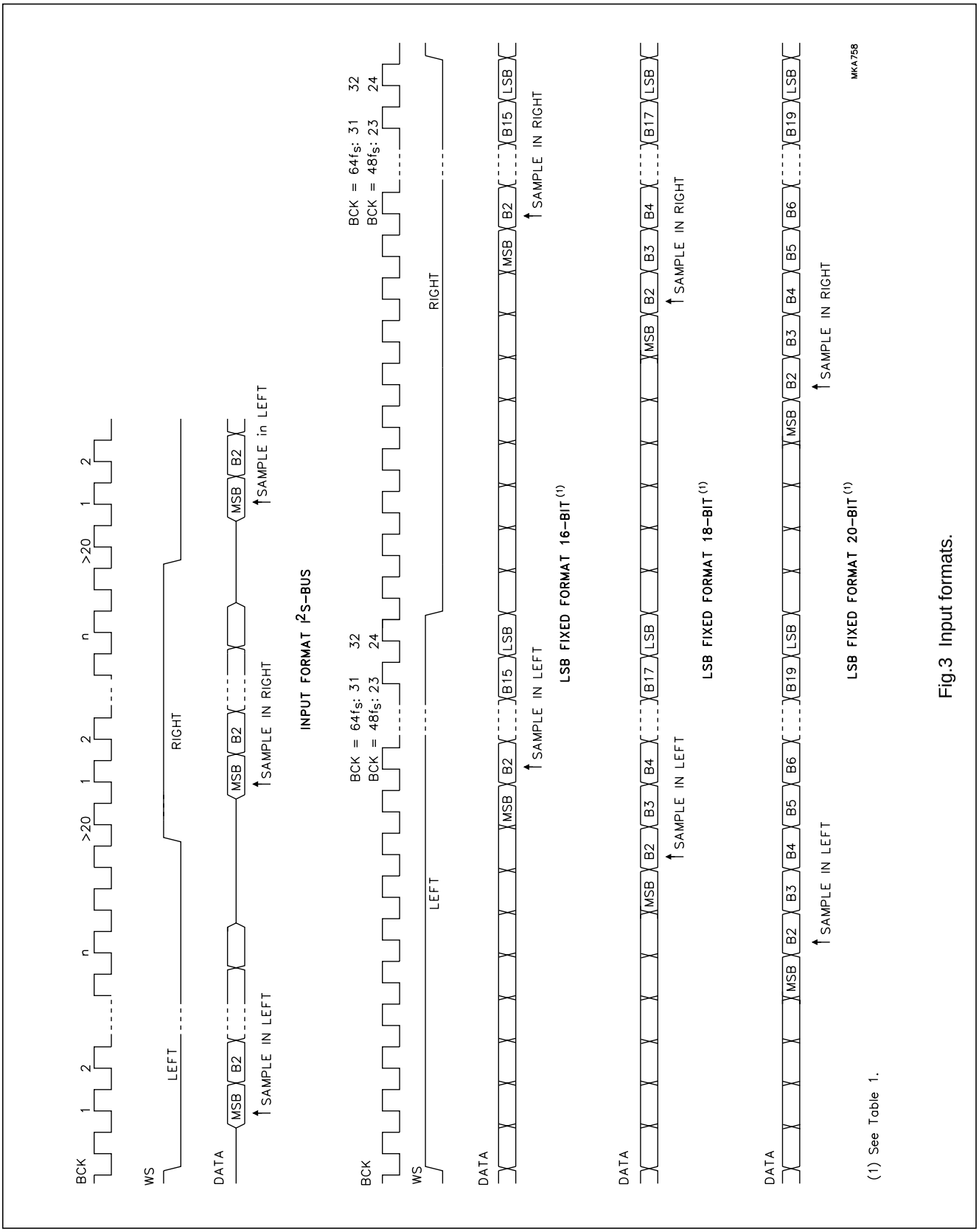
The input format is shown in Fig.3. Left and right data-channel words are time-multiplexed.

Table 1 Data input format and system clock.

TEST1	CLKS1	CLKS2	DATA INPUT FORMAT	SYSTEM CLOCK	DATA CLOCK(1)	SYSCLKO
0	0	0	I^2S up to 20 bits	$256f_s$	>20	$256f_s$
0	0	1	LSB fixed 16 bits	$384f_s$	24	$384f_s$
0	1	0	LSB fixed 18 bits	$384f_s$	24	$384f_s$
0	1	1	LSB fixed 20 bits	$384f_s$	24	$384f_s$
1	0	0	reserved	–	–	–
1	0	1	LSB fixed 16 bits	$384f_s$	32	$384f_s$
1	1	0	LSB fixed 18 bits	$384f_s$	32	$384f_s$
1	1	1	LSB fixed 20 bits	$384f_s$	32	$384f_s$

Note

1. Number of clock pulses within half an audio sample.



(1) See Table 1.

Fig.3 Input formats.

Mute

Soft mute is controlled by the $\overline{\text{MUSB}}$ at pin 9. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. To step down the value of the data 32 coefficients are used, each one being used 31 times before stepping onto the next. When MUTE is released (pin 19 = HIGH), the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order. Mute is synchronized to prevent operation in the middle of a word.

De-emphasis

A digital de-emphasis is implemented for three sample rates (32, 44.1 and 48 kHz). By selecting DEEM1 and DEEM2 de-emphasis can be applied by means of a FIR filter. Time constants of the de-emphasis are 50 μs and 15 μs. De-emphasis is synchronized to prevent operation in the middle of a word. The de-emphasis deviation from ideal 50 μs and 15 μs de-emphasis is given in Table 4.

Table 2 De-emphasis.

DEEM1	DEEM2	CONDITION
0	0	de-emphasis disabled
0	1	de-emphasis for f_s = 32 kHz
1	0	de-emphasis for f_s = 4.1 kHz
1	1	de-emphasis for f_s = 48 kHz

Attenuation

Attenuation is controlled by the $\overline{\text{ATSB}}$ input (pin 21). When the input is active LOW the sample is multiplied by a coefficient that provides 12 dB attenuation. If the input is HIGH the multiplication factor is 1. Attenuation is synchronized to prevent operation in the middle of a word.

Double-speed mode

Double speed is controlled by the $\overline{\text{DSMB}}$ input (pin 20). When the input is active LOW the device operates in the double-speed mode.

Oversampling filter (normal-speed mode)

In the normal-speed mode the oversampling filter consists of:

- A 91st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 23rd order quarter band low-pass FIR filter which increases the oversampling rate from 2 times to 8 times.
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $16f_s$.

Pass-band ripple and stop-band attenuation for normal-speed are given in Table 3.

Oversampling filter (double-speed mode)

In the double-speed mode the oversampling filter consists of:

- A 51st order half-band low-pass FIR filter which increases the oversampling rate from 1 time to 2 times.
- A 7th order half-band low-pass FIR filter which increases the oversampling rate from 2 times to 4 times.
- A linear interpolation section which increases the oversampling rate to 8 times. This removes the spectral components around $4f_s$.
- A sample-and-hold section which provides another 6 times oversampling to 48 times. The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering remove the spectral components around $8f_s$.

Pass-band ripple and stop-band attenuation for double-speed are given in Table 3.

Noise shaper

In the normal speed mode the 2nd order digital noise shaper operates at $96f_s$ ($f_{sys} = 384f_s$) or $128f_s$ ($f_{sys} = 256f_s$). The digital noise shaper operates at $48f_s$ ($f_{sys} = 384f_s$) or $64f_s$ ($f_{sys} = 256f_s$) in double-speed mode. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique used in combination with a special data coding enables extremely high signal-to-noise ratios to be achieved. The noise shaper outputs a 5-bit pulse duration modulation (PDM) bitstream signal to the DAC.

Continuous calibration DAC

The dual 5-bit DAC uses the continuous calibration technique. This method, based on charge storage, involves exact duplication of a single reference current source. In the TDA1305T, 32 such current sources plus 1 spare source are continuously calibrated. The spare source is included to allow continuous converter operation.

The DAC receives a 5-bit data bitstream from the noise shaper. This data is then converted so that only small currents are switched to the output during digital silence (input 00000H). Using this technique extremely high signal-to-noise performance is achieved.

Operational amplifiers

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the converter output current to a voltage capable of driving a line output. This voltage is available at VOL and VOR (1.5 V RMS typical).

Connecting external capacitors CEXT1 and CEXT2 between FILTCL and VOL and between FILTCR and VOR respectively provides the required 1st order post filtering for the left and right channels (see Fig.1). The combinations of R_{CONV1} with CEXT1 and R_{CONV2} with CEXT2 determine the 1st order fall-off frequencies.

Internal reference circuitry

Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.4 to 5.5 V and making the circuit also suitable for battery-powered applications.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	7.0	V
V_{DDA}	analog supply voltage		–	7.0	V
V_{DDO}	operational amplifier supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient operating temperature		–30	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model; C = 100 pF, R = 1500 Ω, V = 2000 V, 3 pulses positive and 3 pulses negative.
2. Machine model; C = 200 pF, R = 10 Ω, L = 0.5 μH.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E"*. The number of this quality specification can be found in the *"Quality Reference Handbook"*. The handbook can be ordered using the code 9398 510 63011.

DIGITAL CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	40	mA
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
RR	ripple rejection to V_{DDA}	note 2	–	25	–	dB
System clock input						
f_{sys}	system frequency	$f_{sys} = 384f_s$	9.6	16.93	18.4	MHz
		$f_{sys} = 256f_s$	6.4	11.29	12.28	MHz
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.8V_{DD}$	–	V_{DD} + 0.5	V
$\lvert I_{LI} \rvert$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
T_{cy}	clock cycle time	$f_{sys} = 384f_s$	104	59.1	54.2	ns
		$f_{sys} = 256f_s$	156	88.6	81.3	ns
Digital inputs; WS, BCK, DATA, $\overline{\text{DSMB}}$, $\overline{\text{MUSB}}$, DEEM1, DEEM2, $\overline{\text{ATSB}}$, CLKS1, CLKS2, TEST1 and TEST2						
V_{IL}	LOW level input voltage	note 3	−0.5	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 3	$0.7V_{DD}$	–	V_{DD} + 0.5	V
$\lvert I_{LI} \rvert$	input leakage current	note 4	–	–	10	µA
C_i	input capacitance		–	–	10	pF
Digital output; CDEC						
V_{OL}	LOW level output voltage	I_{OL} = 0.4 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = −0.2 mA	V_{DD} − 0.5	–	V_{DD}	V
t_r	output rise time	note 5	–	–	20	ns
t_f	output fall time	note 5	–	–	20	ns
C_L	load capacitance		–	–	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial input data timing (see Fig.4)						
f_{BCK}	bit-clock input (data input rate) frequency	$f_{sys} = 384f_s$	–	$48f_s$	–	MHz
		$f_{sys} = 256f_s$	–	$64f_s$	–	MHz
f_{WS}	word select input frequency	normal speed	25	44.1	48	kHz
		double speed	50	88.2	96	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
t_H	bit clock time HIGH		55	–	–	ns
t_L	bit clock time LOW		55	–	–	ns
t_{su}	data set-up time		40	–	–	ns
t_h	data hold time		10	–	–	ns
t_{suWS}	word select set-up time		40	–	–	ns
t_{hWS}	word select hold time		10	–	–	ns

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. V_{ripple} = 1% of supply voltage; f_{ripple} = 100 Hz. Ripple rejection RR to V_{DDA} is dependent on the value of the external capacitor (C_{EXT3} in Fig.1) connected to V_{ref}. The value here assumes that C_{EXT3} = 1 μF.
3. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
4. I_{LImni} measured at V_I = 0 V; I_{LImax} measured at V_I = 5.5 V.
5. Reference levels = 10% and 90%.

ANALOG CHARACTERISTICS

$V_{DD} = V_{DDA} = V_{DDO}$ = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistor		1.6	2.2	2.8	kΩ
Analog outputs						
RES	resolution		–	–	18	bit
$V_{FS(rms)}$	full-scale output voltage (pins 23 and 25) (RMS value)		1.425	1.5	1.575	V
V_{OFF}	output voltage DC offset with respect to reference voltage level V_{ref}		–80	–65	–50	mV
TC_{FS}	full scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 1	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB input level; note 2	–	–44	–40	dB
			–	0.63	1.0	%
		at –60 dB input level; A-weighted; note 3	–	–46	–	dB
			–	0.5	–	%
		at 0 dB input level; (20 Hz to 20 kHz); note 4	–	–90	–81	dB
			–	0.003	0.003	%
S/N	signal-to-noise ratio at bipolar zero	A weighted; at code (00000H)	100	108	–	dB
α_{cs}	channel separation		85	100	–	dB
$\lvert\delta V_O\rvert$	unbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	Ω
R_L	output load resistance		3	–	–	kΩ
C_L	output load capacitance		–	–	200	pF

Notes

1. Measured with a 1 kHz, 0 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.
2. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz. For 16-bit input signals, the performance is limited to the theoretical maximum.
3. Measured with a 1 kHz, -60 dB, 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz and filtered with a A-weighted characteristic. For 16-bit input signals, the performance is limited to the theoretical maximum.
4. Measured with a sine wave from 20 Hz to 20 kHz generated at a sampling rate of 48 kHz. The (THD + N)/S measured over a bandwidth of 20 Hz to 20 kHz.

TEST AND APPLICATION INFORMATION

Filter characteristics (theoretical values)

Table 3 Normal speed filter characteristics.

ITEM	SAMPLE FREQUENCY	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	44.1 kHz	0 to 20 kHz		0 ±0.025 dB
	32 kHz	14.5 to 15 kHz		–0.15 dB (min.)
Stop band	44.1 kHz	24.1 to 150 kHz	typical	–60 dB (max.)
			worst case	–57 dB (max.)
		150 kHz to infinity	typical	–57 dB (max.)
			worst case	–47 dB (max.)
	32 kHz	17 to 17.5 kHz		–40 dB (max.)

De-emphasis filter characteristics (theoretical values)

Table 4 De-emphasis deviation from ideal 50 μs to 15 μs de-emphasis network.

ITEM	SAMPLE FREQUENCY	RANGE	CHARACTERISTICS
Gain deviation	44.1 and 48 kHz	0 to 18 kHz	0 ±0.05 dB
		18 to 20 kHz	0.12 dB (max.)
	32 kHz	0 to 13 kHz	0 ±0.06 dB
		13 to 15 kHz	0.22 dB (max.)
Phase deviation	44.1 and 48 kHz	0 to 15 kHz	10 deg (max.)
		15 to 20 kHz	15 deg (max.)
	32 kHz	0 to 9 kHz	10 deg (max.)
		9 to 15 kHz	16 deg (max.)

Double-speed characteristics

Table 5 Double-speed filter characteristics.

ITEM	RANGE	CONDITIONS	CHARACTERISTICS
Pass band	0 to 17 kHz		0 ±0.075 dB
	17 to 20 kHz		–0.3 dB (min.)
Stop band	24.1 to 150 kHz	typical	–47 dB (max.)
		worst case	–45 dB (max.)
	150 kHz to infinite	typical	–33 dB (max.)
		worst case	–25 dB (max.)

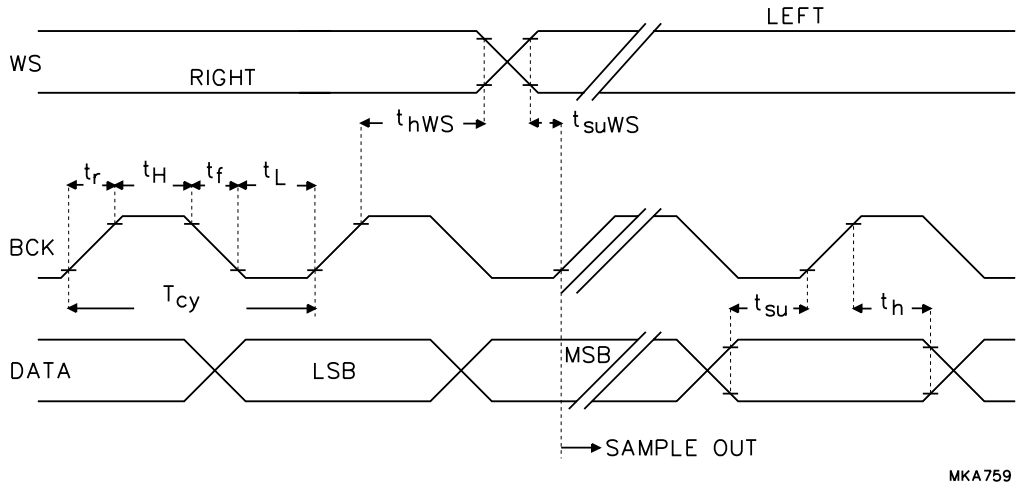


Fig.4 Timing of input signals.

APPLICATION INFORMATION

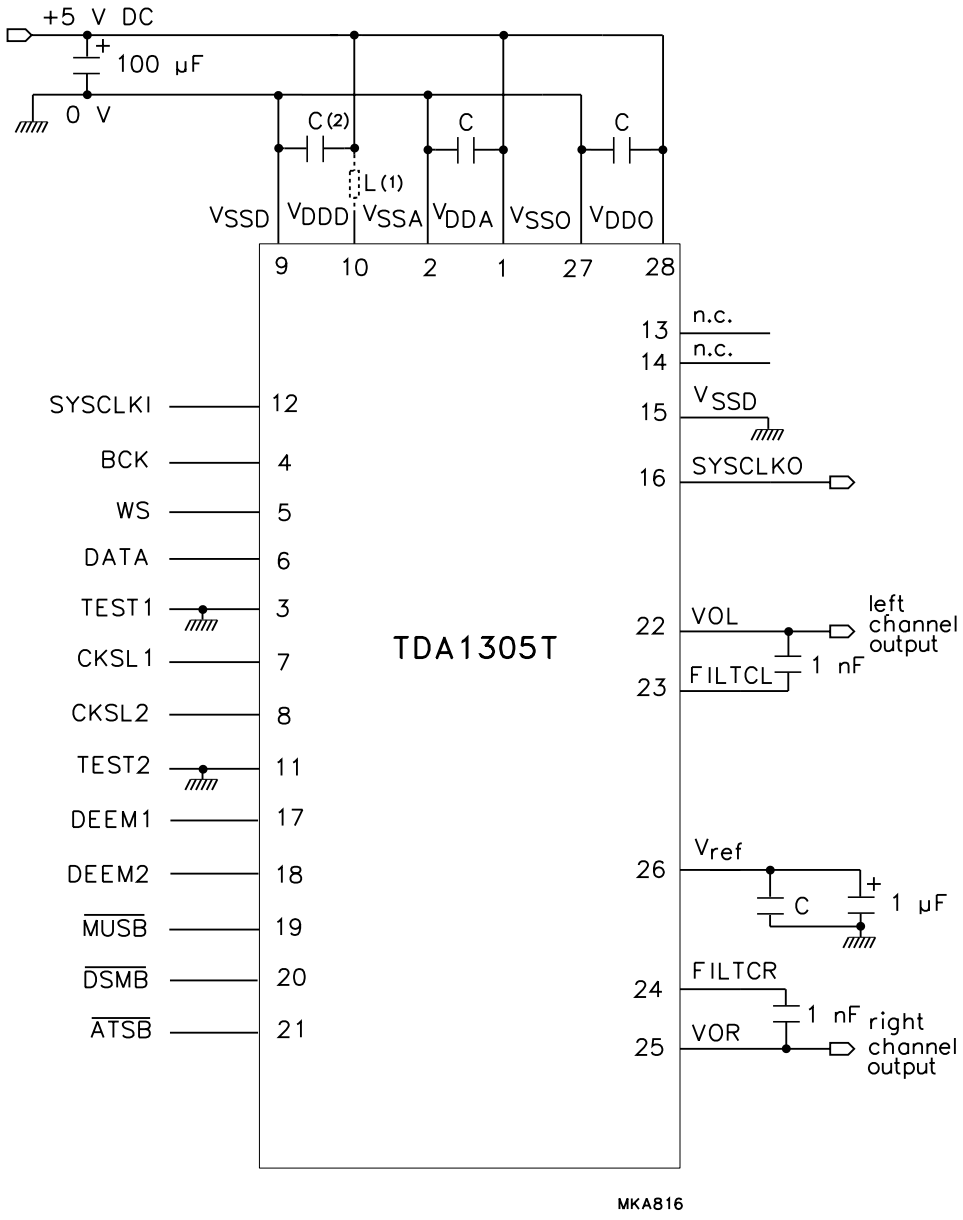
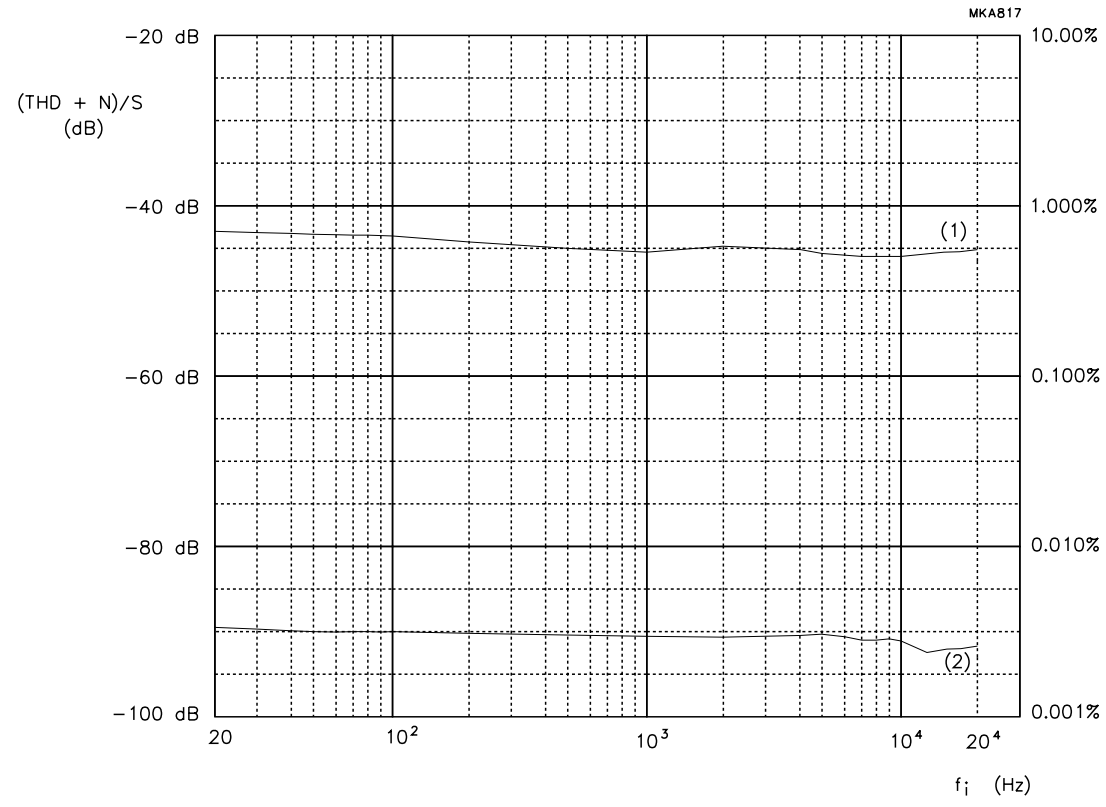


Fig.5 Application diagram.

A typical application diagram is illustrated in Fig.5. The left and right channel outputs can drive a line output directly. The series inductor (L) in the digital supply line, though not strictly necessary, helps to reduce crosstalk between the digital and analog circuits.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

In Fig.6 measurements were taken with an 18-bit sine wave generated at a sampling rate of 48 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz and filtered with A-weighted characteristics. The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.



(1) Level = −60 dB.
(2) Level = 0 dB.

Fig.6 Total harmonic distortion as a function of signal frequency.

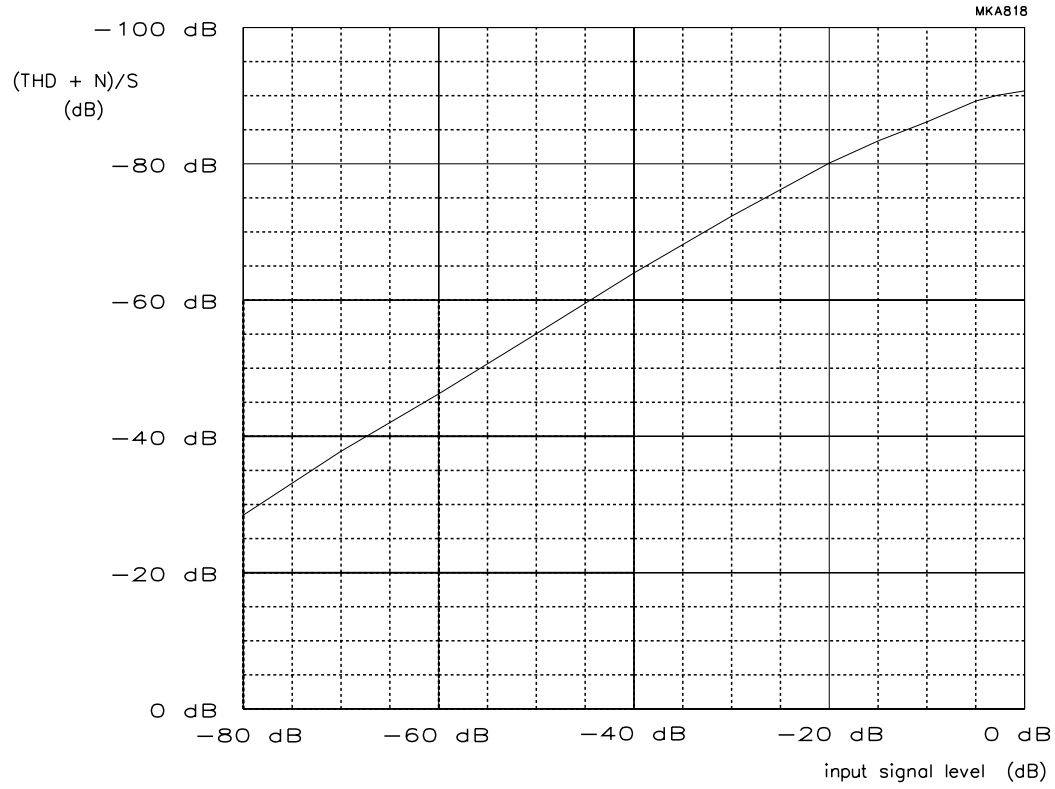
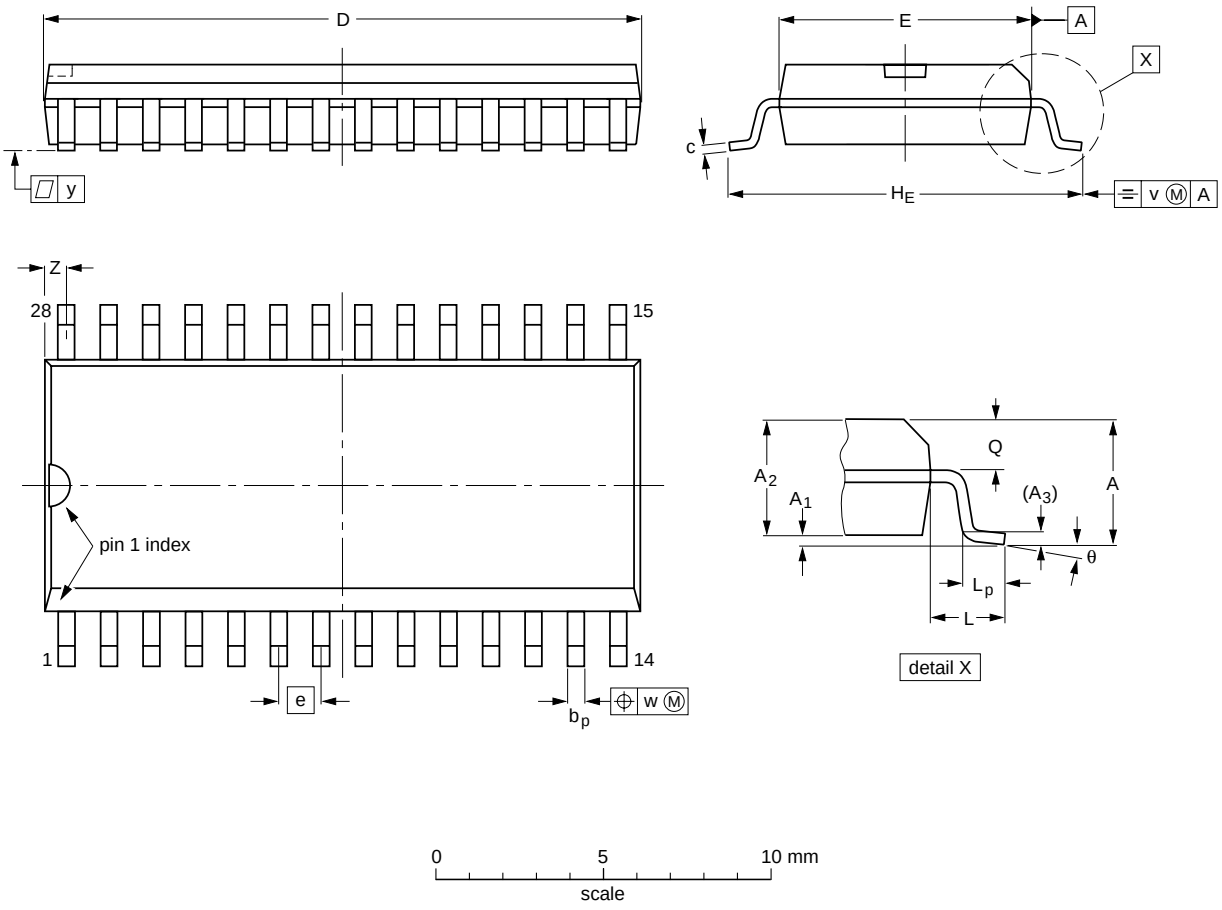


Fig.7 Total harmonic distortion as a function of signal level; (A-weighted).

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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