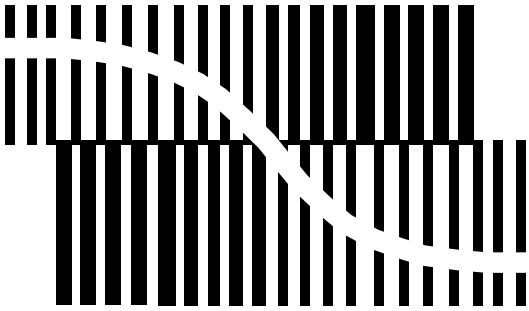
DATA SHEET



TDA1549T

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

Objective specification
File under Integrated Circuits, IC01

August 1994

Philips Semiconductors

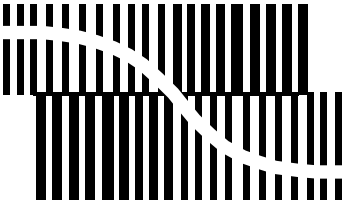
PHILIPS

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

FEATURES

- Easy application
- Finite-duration impulse-response (FIR) filtering and noise shaping incorporated
- 2nd-order noise shaper
- Wide dynamic range (true 18-bit resolution)
- Low total harmonic distortion
- No zero-crossing distortion
- Superior signal-to-noise ratio
- Bitstream continuous calibration conversion concept
- Inherently monotonic
- Voltage output (1.5 V RMS) at line drive level
- Single supply rail (3.8 to 5.5 V)
- Optimum output voltage level over the entire supply range
- Small outline packaging (SO16)
- Wide operating temperature range (–30 to +85 °C)
- Standard Japanese input format
- No analog post-filtering required
- Low power consumption
- Integrated operational amplifiers.



GENERAL DESCRIPTION

The TDA1549T (BCC-DAC1) is the first of a new generation of digital-to-analog converters featuring a unique combination of bitstream and continuous calibration concepts.

A system of digital filtering, high oversampling, 2nd order noise shaping and continuous calibration digital-to-analog conversion ensures that only simple 1st order analog filtering is required. The circuit accepts 18-bit four times oversampled input data ($4f_s$) in standard Japanese format. Internal FIR filters remove the main spectral components and increase the sampling rate to 96 times ($96f_s$). A 2nd order noise shaper converts this oversampled data to a 5-bit data stream. For low signal levels the converter operates in the 1-bit bitstream mode with attendant high differential linearity. Higher level signals are reproduced using the dynamic continuous calibration technique, thereby guaranteeing high linearity independent of process variations, temperature effects and product ageing.

High-precision, low-noise amplifiers convert the digital-to-analog current to an output voltage capable of driving a line output. Externally connected capacitors perform the required 1st order filtering so that no further post-filtering is required.

Internal reference circuitry ensures that the output voltage is proportional to the supply voltage, thereby making optimum use of the supply voltage over a wide range (3.8 to 5.5 V). This unique configuration of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a digital-to-analog conversion system with true 18-bit dynamic range, high linearity and simple low-cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1549T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162–1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	12	18	mA
I_{DDA}	analog supply current	note 2	–	5.5	8	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	9	mA
P_{tot}	total power dissipation	note 2	–	120	185	mW
		note 3	–	50	–	mW
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V	1.425	1.500	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–83	dB
			–	0.003	0.007	%
		at –60 dB signal level	–	–48	–40	dB
			–	0.40	1.0	%
		at –60 dB signal level; A-weighted	–	–50	–	dB
			–	0.38	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	110	–	dB
t_{cs}	current setting time to ±1 LSB		–	0.1	–	µs
BR	input bit rate at data input		–	–	9.216	Mbits
f_{BCK}	input clock frequency		–	–	9.216	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. All V_{DD} and ground pins must be connected externally to the same supply.
2. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 5 V at input data code 00000H.
3. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 3.8 V at input data code 00000H.

BLOCK DIAGRAM

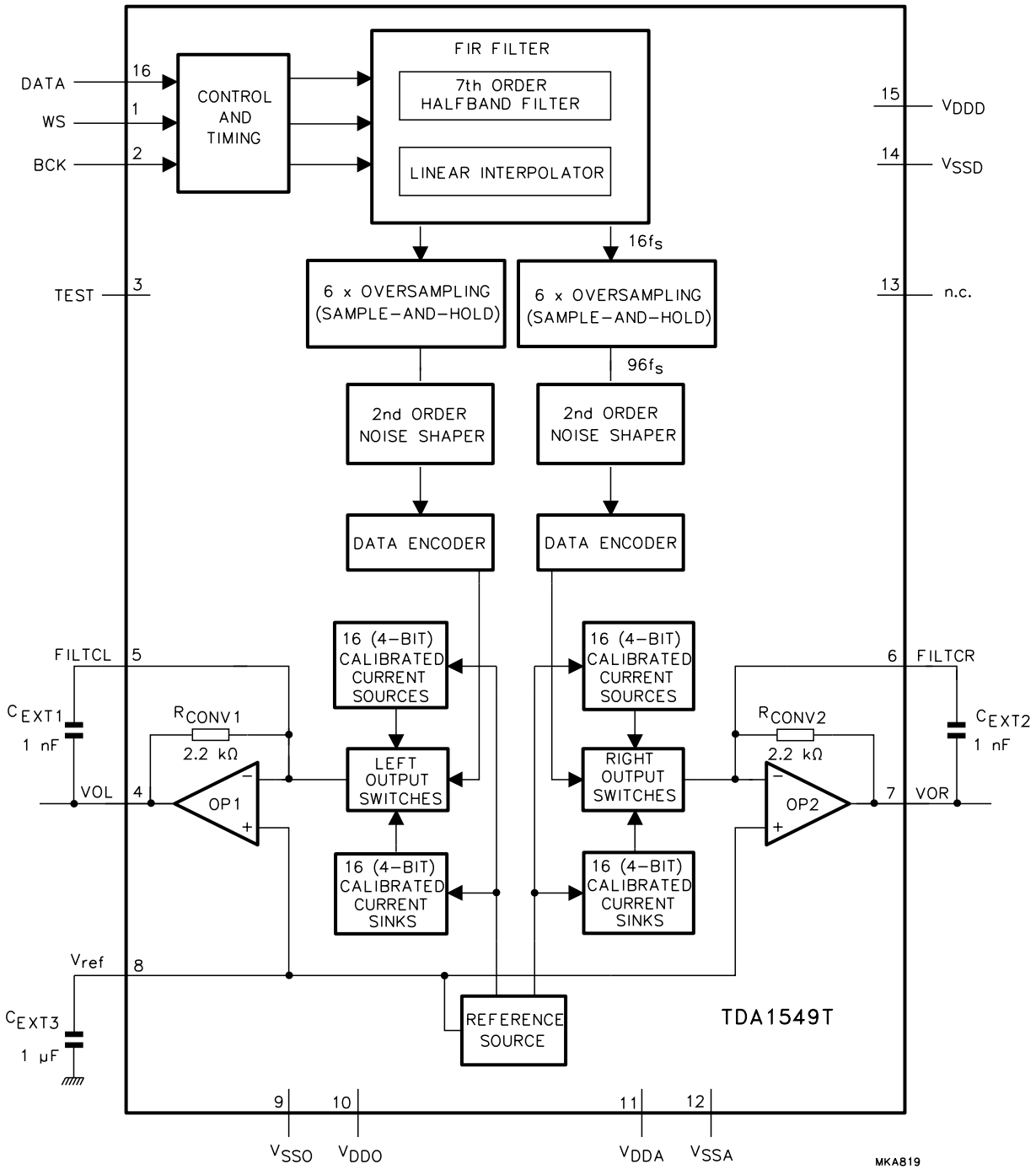


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WS	1	word select input
BCK	2	bit clock input
TEST	3	test input; pin should be connected to ground
VOL	4	left channel output
FILTCL	5	capacitor for left channel 1st order filter function; should be connected between pins 4 and 5
FILTCR	6	capacitor for right channel 1st order filter function; should be connected between pins 6 and 7
VOR	7	right channel output
V_{ref}	8	internal reference voltage for output channels ($\frac{1}{2}V_{DD}$)
V_{SSO}	9	operational amplifier ground
V_{DDO}	10	operational amplifier supply voltage
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected (this pin should be left open-circuit)
V_{SSD}	14	digital ground
V_{DDD}	15	digital supply voltage
DATA	16	data input

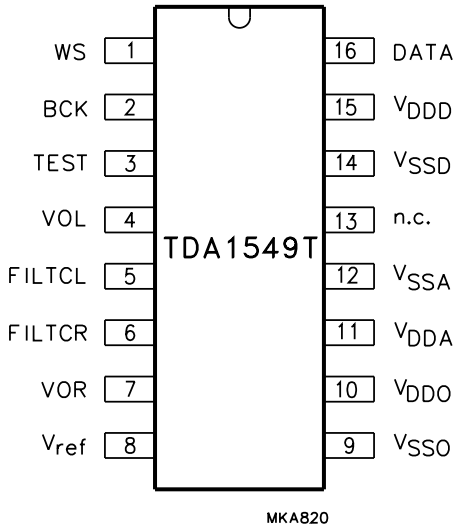


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The TDA1549T CMOS digital-to-analog bitstream continuous calibration converter incorporates internal digital filtering which increases the oversampling rate of $4f_S$ input data to $96f_S$, and removes the spectral data components around $4f_S$, $8f_S$, and $12f_S$. A 2nd order noise shaper operating at $96f_S$ outputs a 5-bit data bitstream to the DACs. The filtering required for waveform smoothing and out-of-band noise reduction is achieved by simple 1st order analog post-filtering (see Fig.3).

The combination of noise shaping and bitstream continuous calibration digital-to-analog conversion enables high performance and extremely low noise to be achieved.

Input

The circuit accepts four times oversampled data in 18-bit two's complement standard Japanese format with MSB first. Left and right data channel words are time multiplexed. The input format is illustrated in Fig.5. The bit clock (BCK) operates at $192f_S$, i.e. 48 times the word select (WS) frequency of $4f_S$.

Oversampling filter

The oversampling filter consists of:

- A 7th order half-band low-pass FIR filter which increases the oversampling rate from 4 times to 8 times. This removes the spectral components around $4f_S$ and $12f_S$ (see Fig.3).
- A linear interpolation section which increases the oversampling rate to 16 times. This removes the spectral components around $8f_S$.
- A sample-and-hold section which provides another 6 times oversampling to 96 times.

The zero-order hold characteristic of this sample-and-hold section plus the 1st order analog filtering removes the spectral components around $16f_S$.

Passband ripple is within 0.1 dB. Stopband attenuation is >50 dB around multiples of the sampling frequency.

Noise Shaper

The 2nd-order digital noise shaper converts the 18-bit data at $96f_S$ into a 5-bit bitstream, while shifting in-band quantization noise to frequencies well above the audio band. For low signal levels the noise shaper output is a 1-bit bitstream. This noise shaping technique used in combination with a special data code and bitstream DAC enables extremely high signal-to-noise ratios to be achieved.

Data encoder

The data encoder converts the 5-bit two's complement output data from the noise shaper to a 32-bit thermometer code.

In traditional unidirectional current converters, half of the full-scale current flows to the output during small signal reproduction. The thermal noise and substrate crosstalk components present in this current severely restrict the dynamic range which can be attained. In this BCC-DAC1 true low-noise performance is achieved using a special data code and bidirectional current sources. The special data code guarantees that only small values of current flow to the output during small-signal passages while larger positive or negative signals are generated using the bidirectional current sources. For every change in the 18-bit input sample only one current source or current sink is switched on. This intrinsically monotonic thermometer code ensures the high differential linearity, zero crossover distortion and superior signal-to-noise ratio associated with bitstream conversion.

Continuous calibration DAC

The stereo 5-bit DAC uses the dynamic continuous calibration technique. The DAC currents (16 sources and 16 sinks) of each channel are repeatedly generated from one single reference current. This duplication is based on an internal charge storage principle and has an inherently high accuracy which is insensitive to ageing, temperature and process variations.

Figure 4 shows one such current calibration source. During calibration the cell is connected to the reference current sink I_{ref} via switch S2. The calibration transistor M1 is connected as an MOS diode via the switch S1 forcing its gate potential to assume a value so that the total current of the calibration cell is equal to the reference current. After calibration the gate of M1 is allowed to float. The gate capacitance C_{gs} retains its potential and the current through the cell remains exactly equal to the reference current. This current is now connected to the output. Each digital-to-analog current source and each current sink is calibrated precisely in this way.

Operational amplifiers

High precision, low-noise amplifiers together with the internal conversion resistors R_{CONV1} and R_{CONV2} convert the DAC output current to a voltage capable of driving a line output. This voltage is available at VOL and VOR (1.5 V RMS typical).

Connecting external capacitors C_{EXT1} and C_{EXT2} between FILTCL and VOL and FILTCR and VOR respectively, provides the required 1st-order post-filtering for the left and right channels (see Fig.1). The combinations of R_{CONV1} with C_{EXT1} and R_{CONV2} with C_{EXT2} determine the 1st order fall-off frequencies.

Internal reference circuitry

Internal reference circuitry ensures that the output voltage signal is proportional to the supply voltage, thereby maintaining maximum dynamic range for supply voltages from 3.8 to 5.5 V and making the circuit also suitable for battery-powered applications.

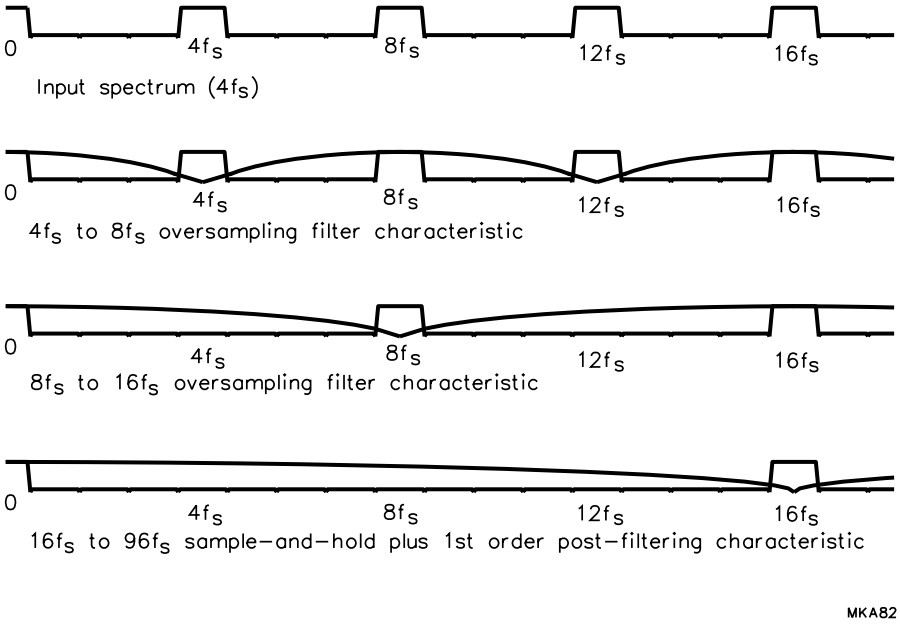
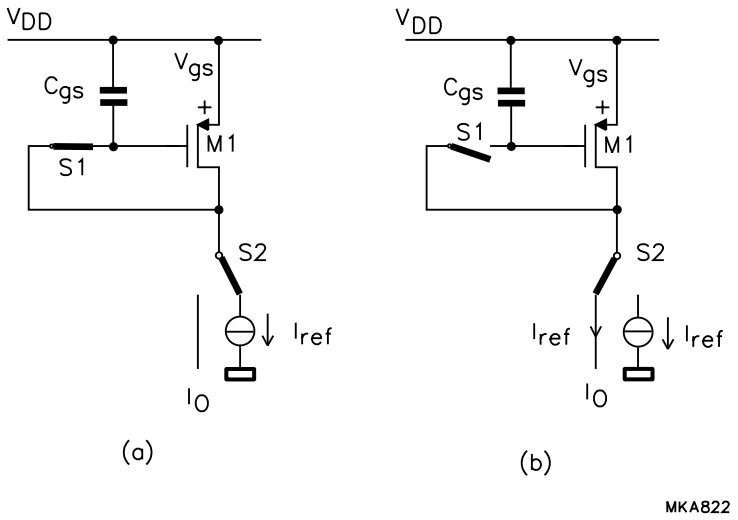


Fig.3 Filter and noise shaper characteristics.



(a) calibration.
(b) operation.

Fig.4 Calibration principle.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–	7.0	V
V_{DDA}	analog supply voltage		–	7.0	V
V_{DDO}	operational amplifier supply voltage		–	7.0	V
T_{xtal}	maximum crystal temperature		–	+150	°C
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–30	+85	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: C = 100 pF; R = 1500 Ω.
2. Machine model: C = 200 pF; L = 0.5 μH; R = 10 Ω.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

QUALITY SPECIFICATION

Quality specification in accordance with "*SNW-FQ-611*" is applicable.

CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	12	18	mA
I_{DDA}	analog supply current	note 2	–	5.5	8	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	9	mA
P_{tot}	total power dissipation	note 2	–	120	185	mW
		note 3	–	50	–	mW
RR	ripple rejection	note 4	–	25	–	dB
Digital inputs; pins WS, BCK and DATA						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
V_{IL}	LOW level input voltage		–0.5	–	$0.3V_{DD}$	V
$\|I_{LIH}\|$	HIGH level input leakage current	$V_{IH} = V_{DDD} = 5$ V	–	–	10	µA
$\|I_{LIL}\|$	LOW level input leakage current	$V_{IH} = V_{SSD} = 0$ V	–	–	10	µA
C_I	input capacitance		–	–	10	pF
Timing (see Fig.6)						
OPERATING FREQUENCY						
f_{BCK}	bit clock frequency		–	$192f_s$	–	Hz
f_{WS}	word select frequency		–	$f_{BCK}/48$	–	Hz
INPUT FREQUENCY						
f_{BCK}	clock frequency		–	–	9.216	MHz
BR	bit rate data input		–	–	9.216	MHz
f_{WS}	word select input frequency		–	–	192	kHz
t_r	rise time		–	–	32	ns
t_f	fall time		–	–	32	ns
T_{cy}	bit clock cycle time		108	–	–	ns
t_H	bit clock HIGH time		22	–	–	ns
t_L	bit clock LOW time		22	–	–	ns
t_{su}	data set-up time		32	–	–	ns
t_h	data hold time		2	–	–	ns
t_{hWS}	word select hold time		2	–	–	ns
t_{suWS}	word select set-up time		32	–	–	ns
Filter characteristics (see Fig.3)						
PBR	pass-band ripple	< 20 kHz	–	0.1	–	dB
SBA	stop-band attenuation	note 5	50	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference values						
V_{ref}	reference voltage level		2.45	2.5	2.55	V
R_{CONV}	current-to-voltage conversion resistance		1.6	2.2	2.8	kΩ
Analog outputs; pins VOL and VOR						
RES	resolution		–	–	18	bit
$V_{FS(rms)}$	full-scale output voltage (RMS value)		1.425	1.5	1.575	V
V_{OFF}	output voltage DC offset with respect to reference voltage level V_{ref}		–80	–65	–50	mV
TC_{FS}	full-scale temperature coefficient		–	$\pm 100 \times 10^{-6}$	–	
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB input level; note 6	–	–90	–83	dB
			–	0.003	0.007	%
		at –60 dB input level; note 7	–	–48	–40	dB
			–	0.40	1.0	%
		at –60 dB input level; A-weighted; note 8	–	–50	–	dB
			–	0.32	–	%
		at 0 dB input level; 20 Hz to 20 kHz; note 9	–	–90	–83	dB
			–	0.003	0.007	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	110	–	dB
t_{cs}	current setting time to ±1 LSB		–	0.1	–	ms
α_{cs}	channel separation		85	100	–	dB
$\lvert\Delta V_O\rvert$	unbalance between outputs		–	0.2	0.3	dB
$\lvert Z_O\rvert$	dynamic output impedance		–	10	–	W
R_L	output load resistance		3	–	–	kΩ
C_L	output load capacitance		–	–	200	pF

Notes

1. All V_{DD} and V_{SS} pins must be connected externally to the same supply.
2. Measured with $V_{DDD} = V_{DDA} = V_{DDO} = 5$ V at input data code 00000H.
3. Measured with $V_{DDD} = V_{DDA} = V_{DDO} = 3.8$ V at input data code 00000H.
4. V_{ripple} = 1% of the supply voltage and f_{ripple} = 100 Hz. Ripple rejection RR to V_{DDA} is dependent on the value of the external capacitor (C_{EXT3} in Fig.1) connected to V_{ref}. The value quoted here assumes C_{EXT3} = 1 μF.
5. Around multiples of 4f_s.
6. Measured with a 1 kHz, 0 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.
7. Measured with a 1 kHz, –60 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.
8. Measured with a 1 kHz, –60 dB, 18-bit sine wave generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz and filtered with A-weighted characteristic.
9. Measured with a 0 dB, 18-bit sine wave from 20 Hz to 20 kHz generated at a sampling rate of 192 kHz. (THD + N)/S measured over a bandwidth from 20 Hz to 20 kHz.

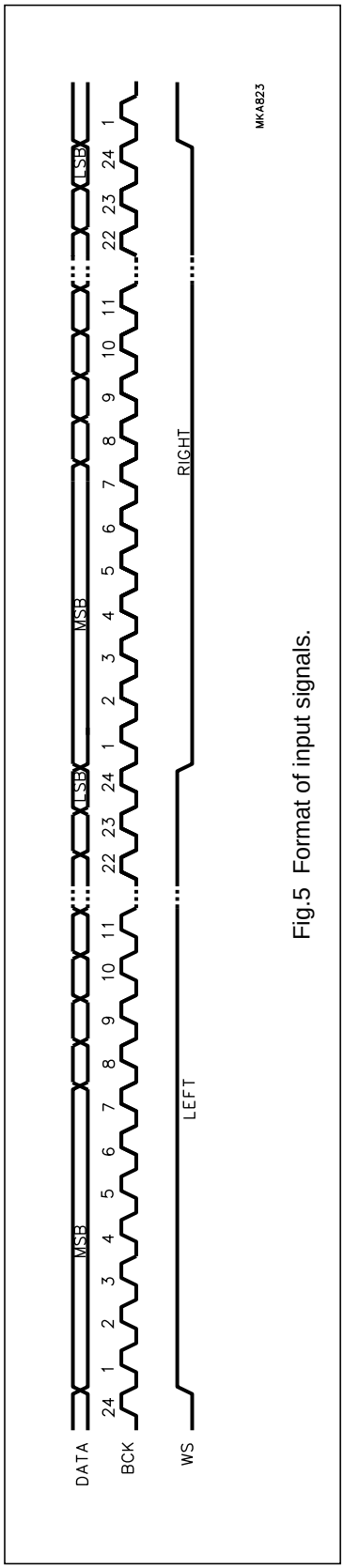


Fig.5 Format of input signals.

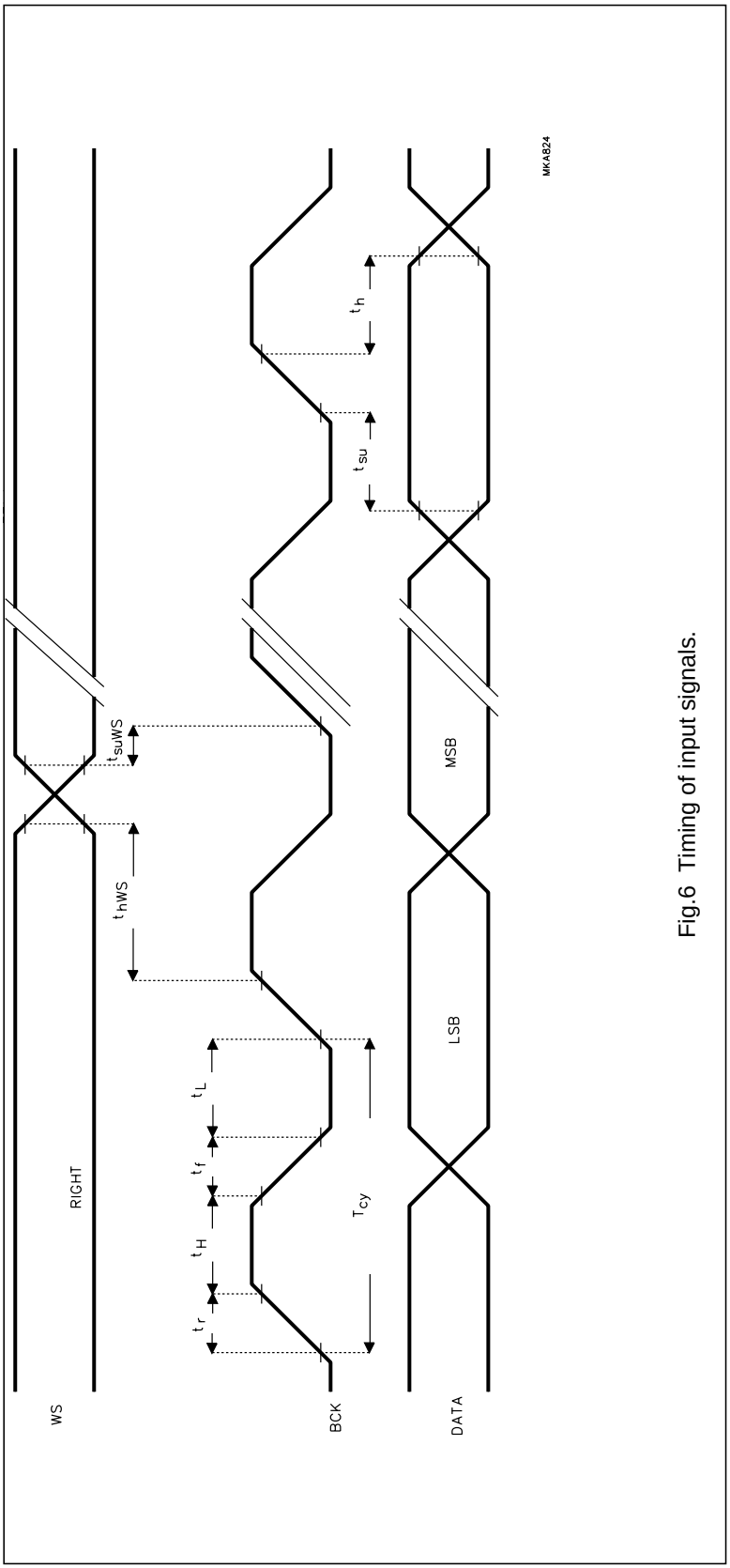
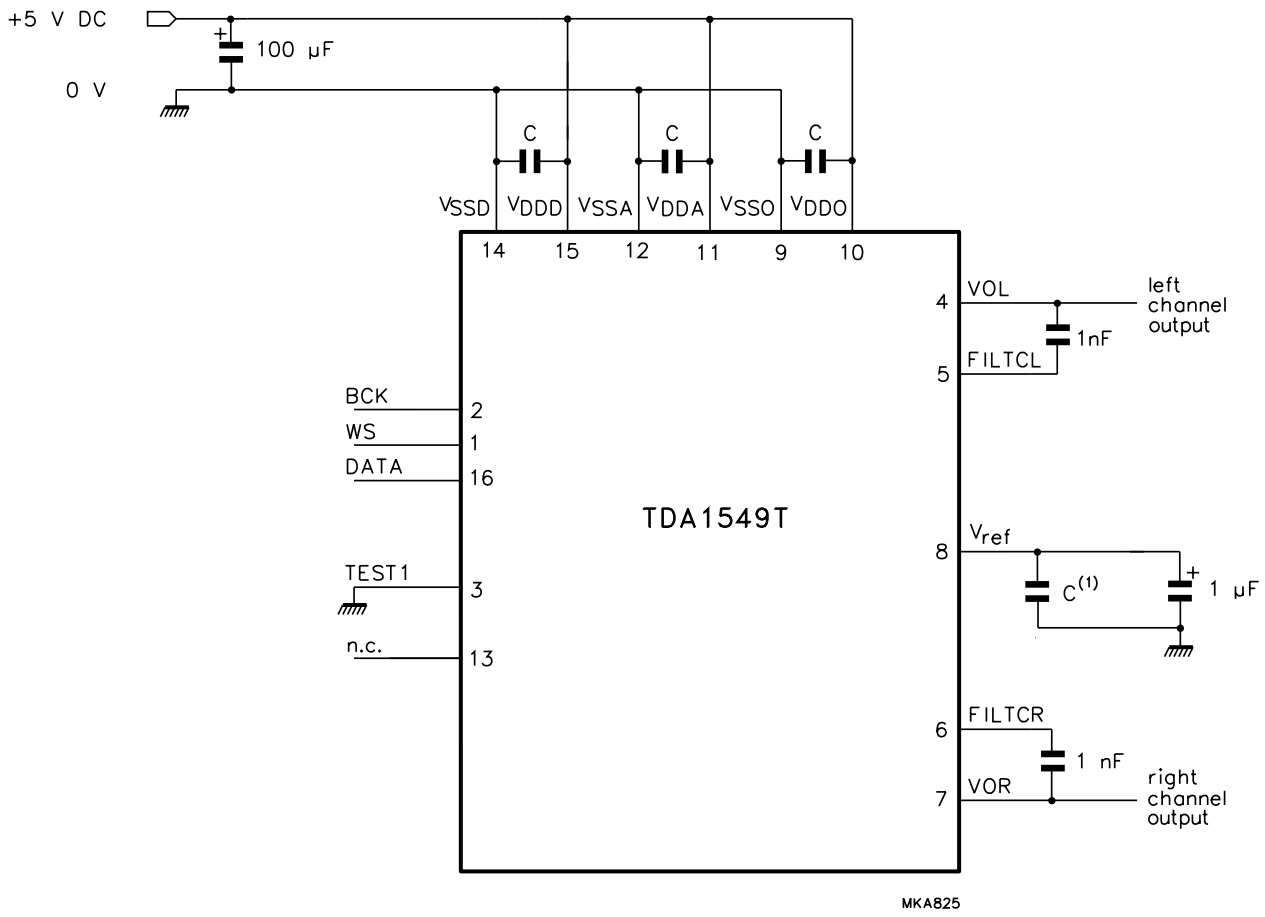


Fig.6 Timing of input signals.

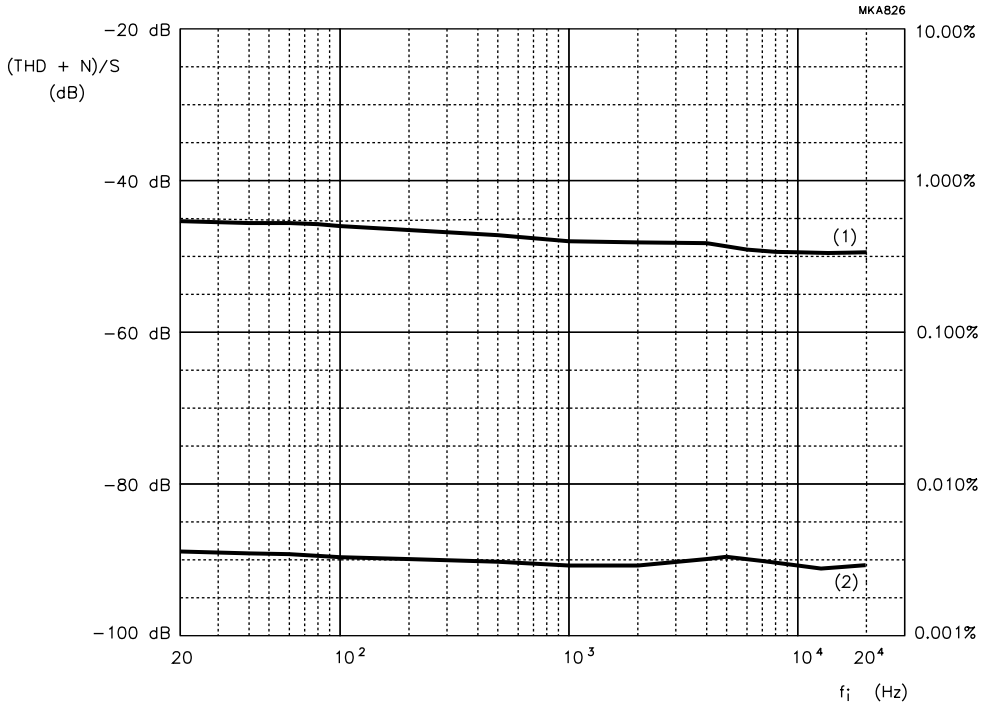
APPLICATION INFORMATION

A typical application diagram is illustrated in Fig.7. The left and right channel outputs can drive a line output directly.



(1) C = 100 nF (chip capacitor).

Fig.7 Application diagram.



(1) Level = −60 dB.
(2) Level = 0 dB.

Fig.8 Total harmonic distortion plus noise-to-signal ratio as a function of signal frequency.

In Fig.8 measurements were taken with an 18-bit sine wave generated at a sample rate of 192 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz.

The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

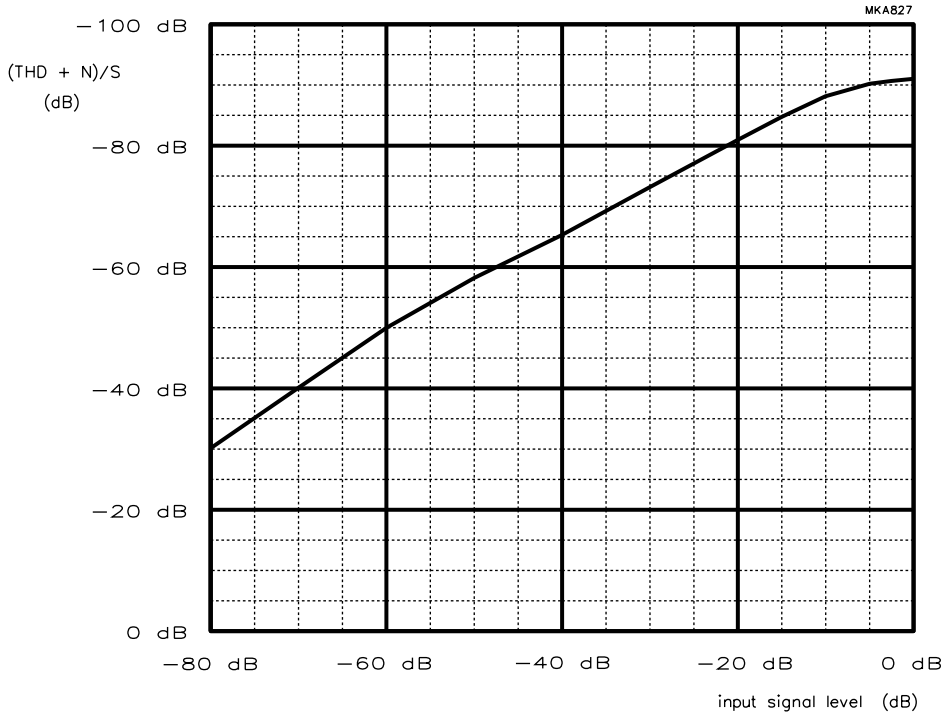
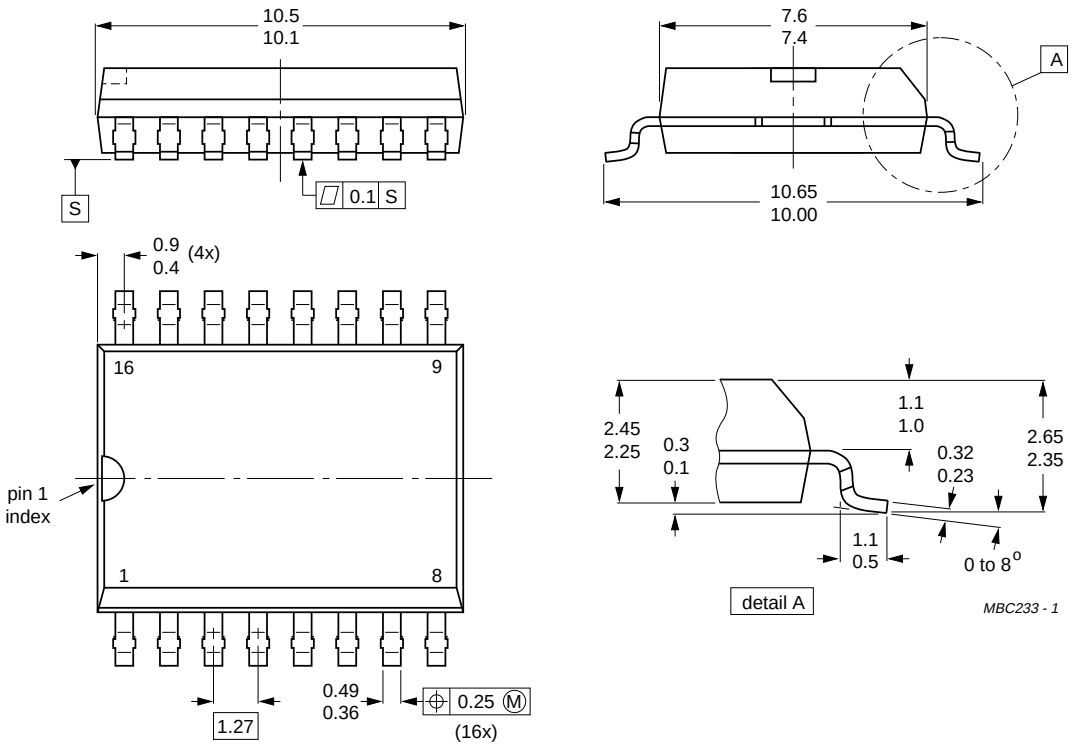


Fig.9 Total harmonic distortion plus noise-to-signal ratio as a function of signal level; (A-weighted).

In Fig.9 measurements were taken with an 18-bit sine wave generated at a sample rate of 192 kHz. The (THD + N)/S was measured over a bandwidth of 20 Hz to 20 kHz and filtered with A-weighted characteristic.

The graph was constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

PACKAGE OUTLINE



Dimensions in mm.

Fig.10 Plastic small outline package; 16 leads; body width 7.5 mm; (SO16; SOT162-1).

SOLDERING

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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